# Transparent Memory Encryption and Authentication

**Mario Werner, *Thomas Unterluggauer*, Robert Schilling, David Schaffenrath, and Stefan Mangard,**
**IAIK, Graz University of Technology**

6. September 2017

# Content

- FPGA security: attackers with physical access
- IP protection: secure boot, FPGA bitfile encryption

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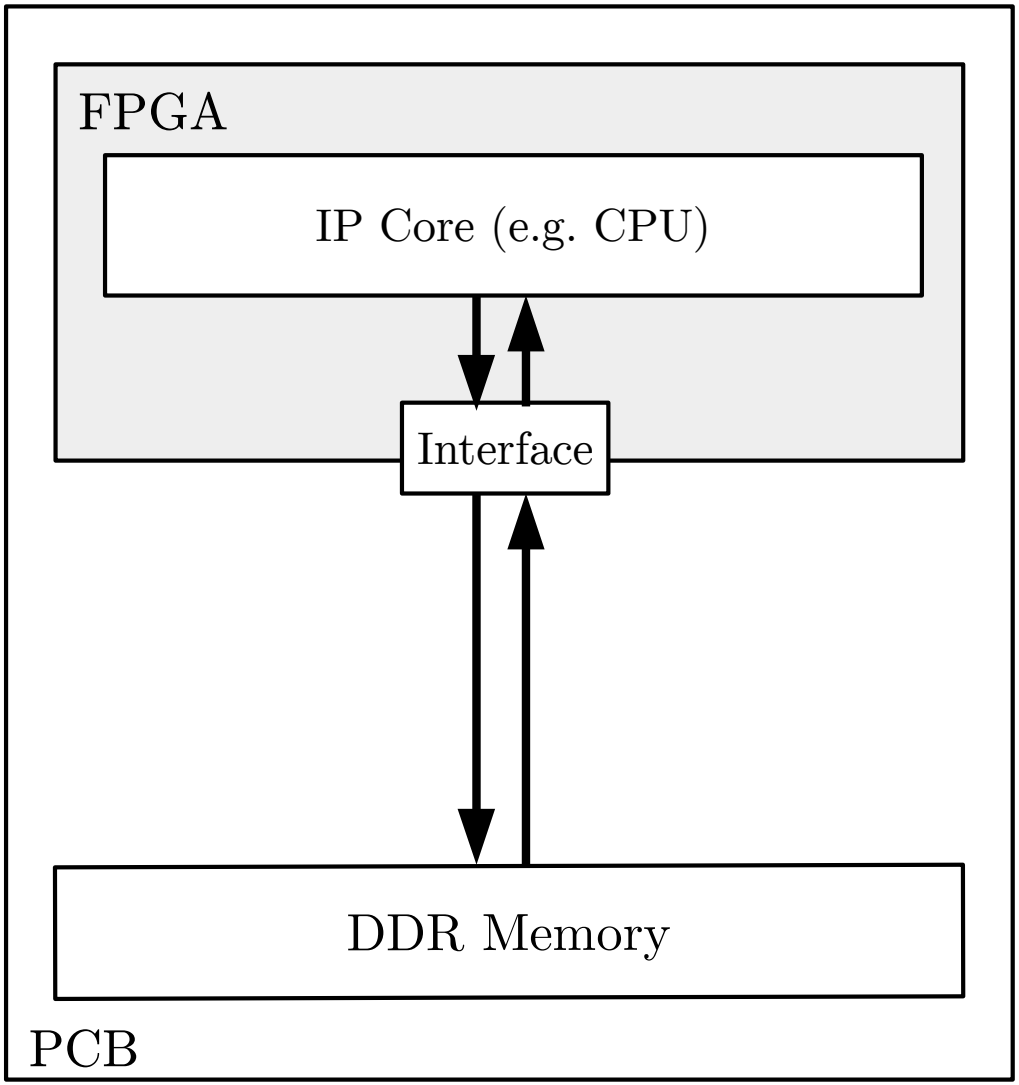
- Missing protection for runtime data in RAM
- Open-source framework for RAM encryption and authentication
  - Supports various cipher modes, e.g., AES-XTS
  - Evaluation on Xilinx Zynq-7020 SoC @ 50 MHz
  - Efficient pipeline: up to 187 MB/s
    - FPGA bus interface limit: 200 MB/sec
  - Authenticated encryption ASCON: 105 MB/s

# Motivation



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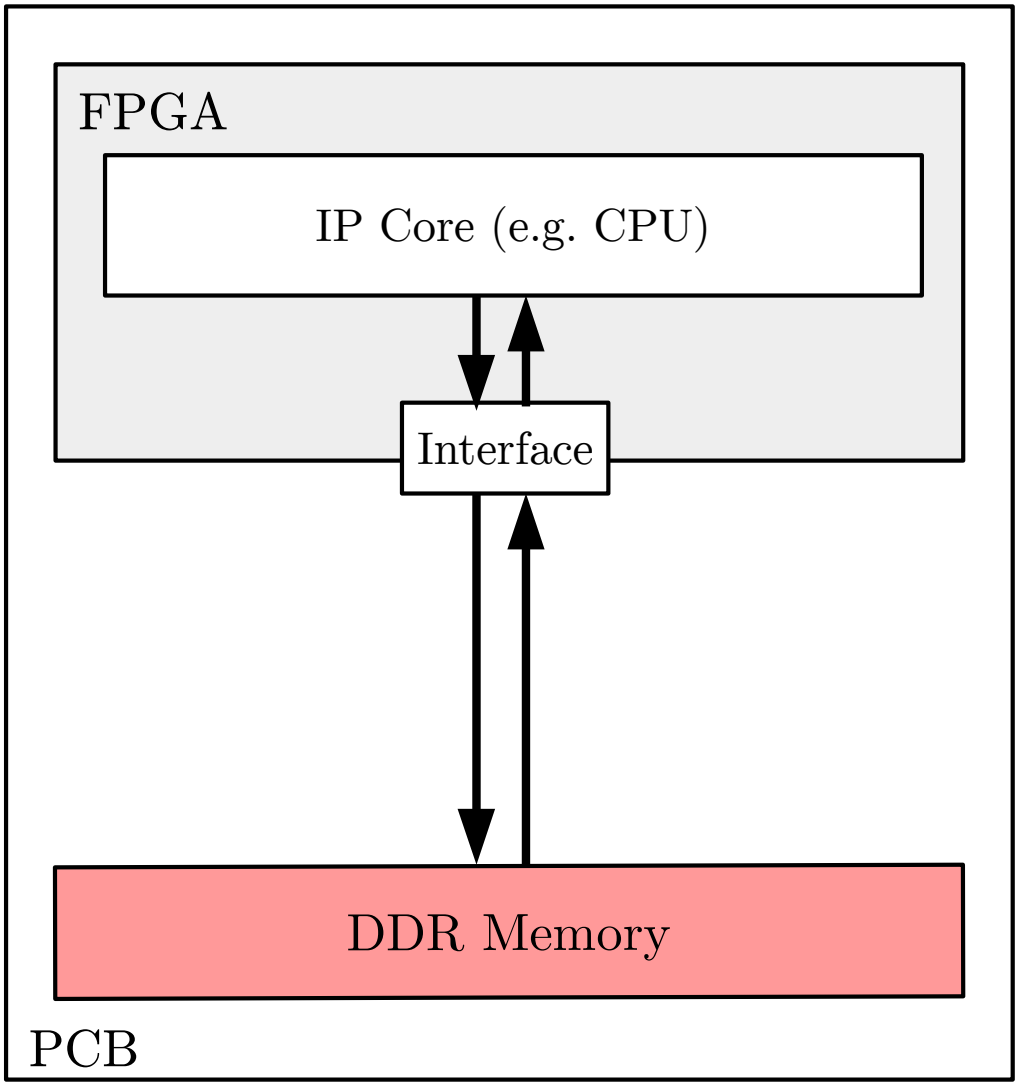

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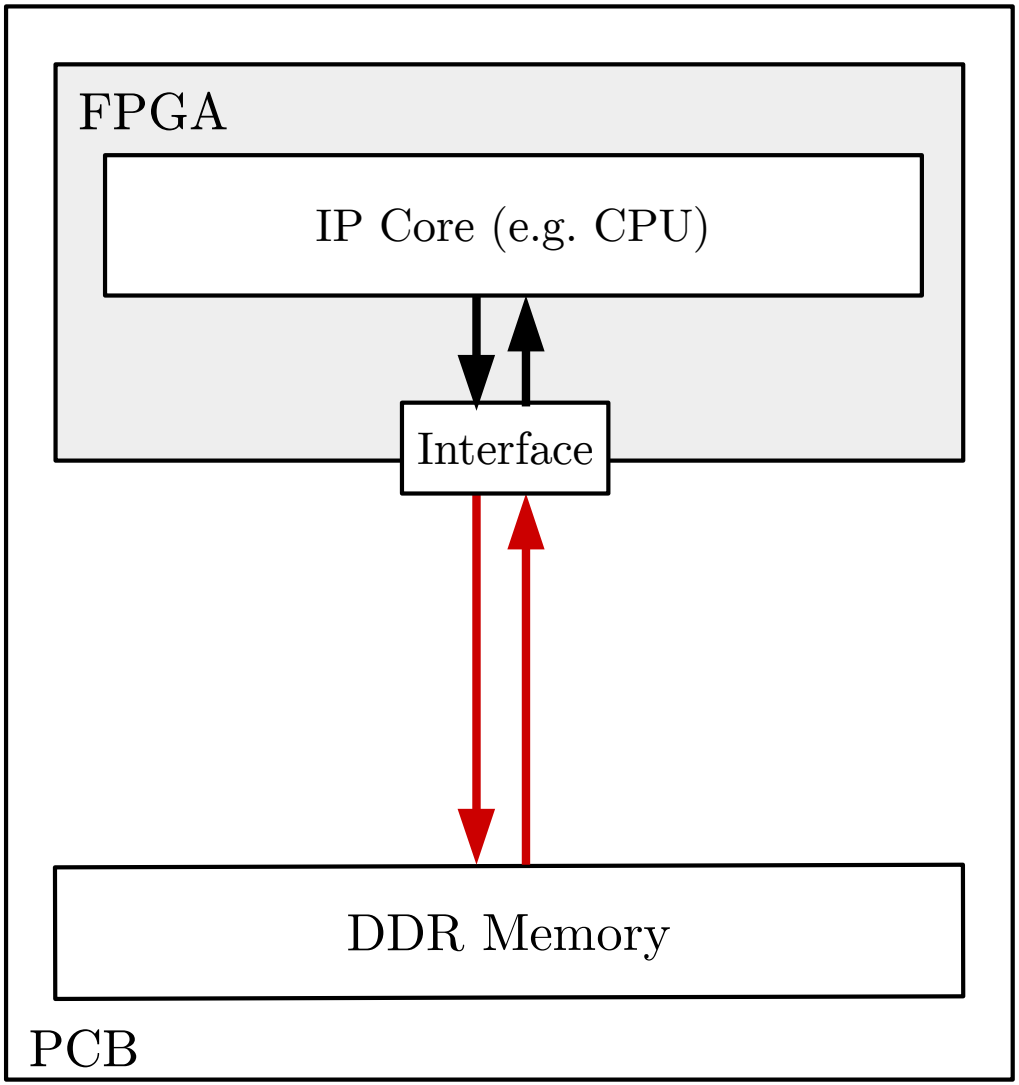
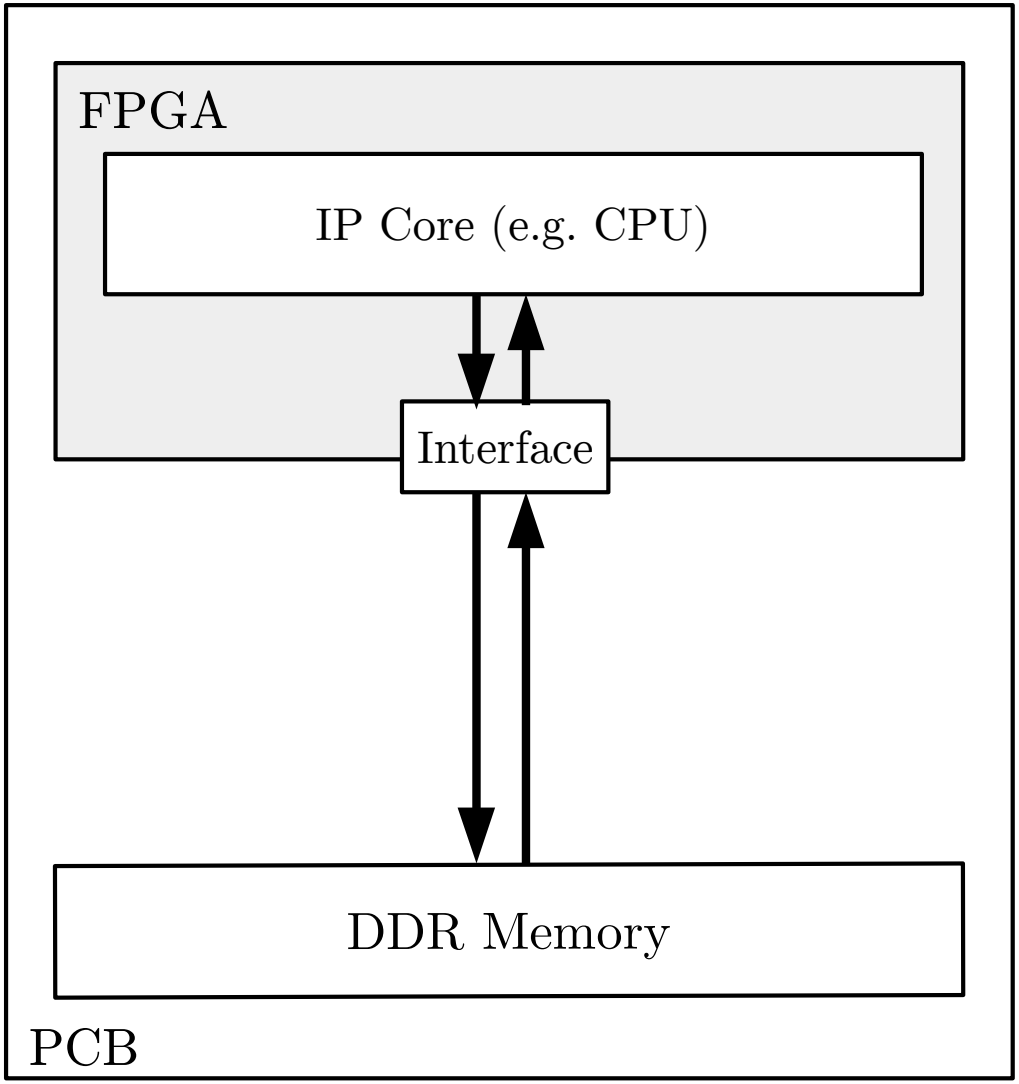


# Motivation

- RAM holds sensitive information and IP
- Hardly any protection of RAM during runtime
- **Need for encryption and authentication of RAM**

# Generic Concept



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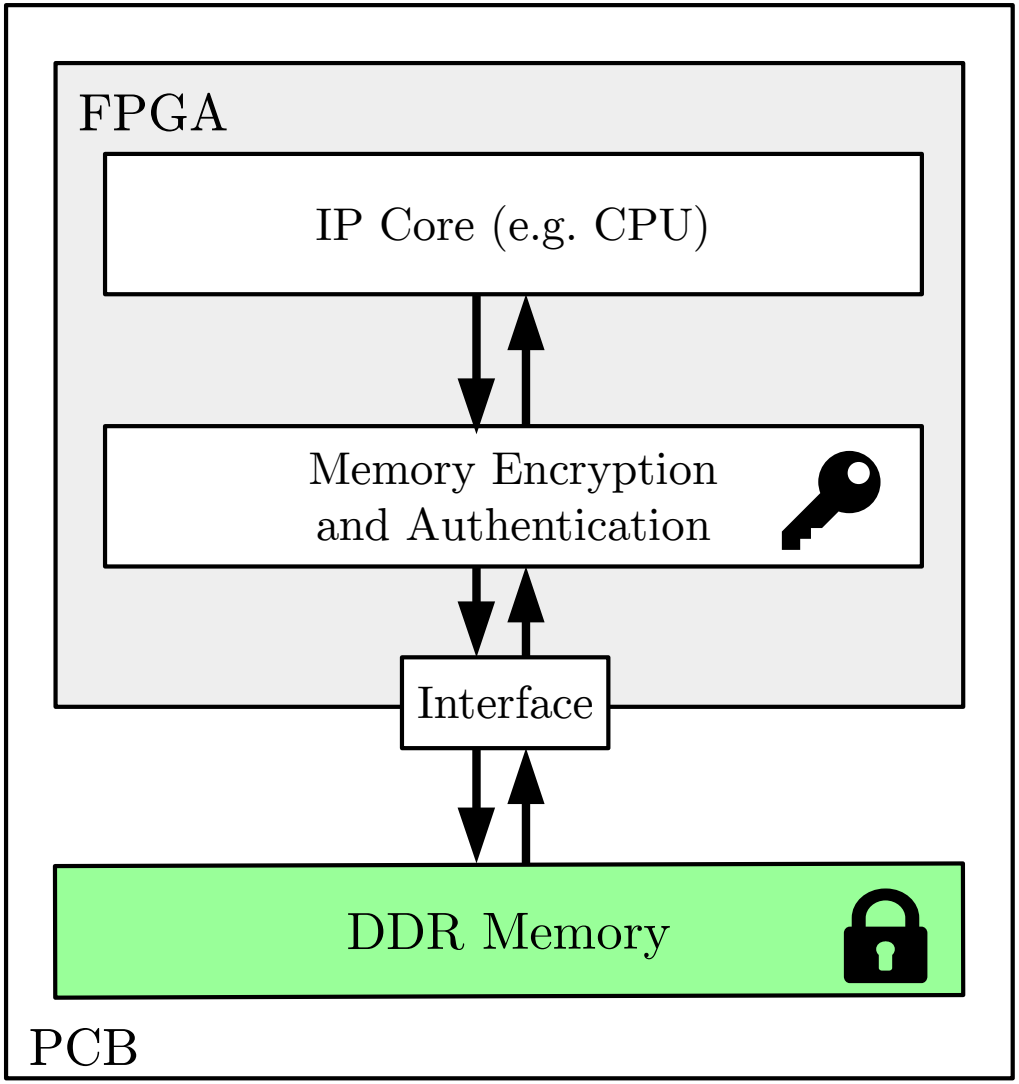

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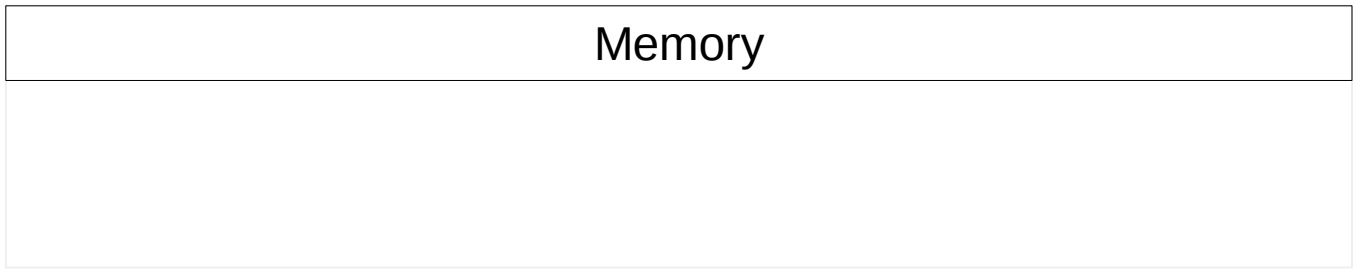

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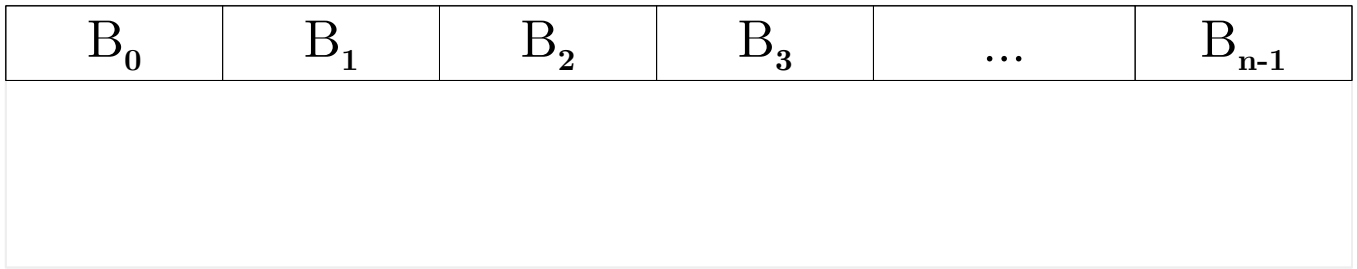

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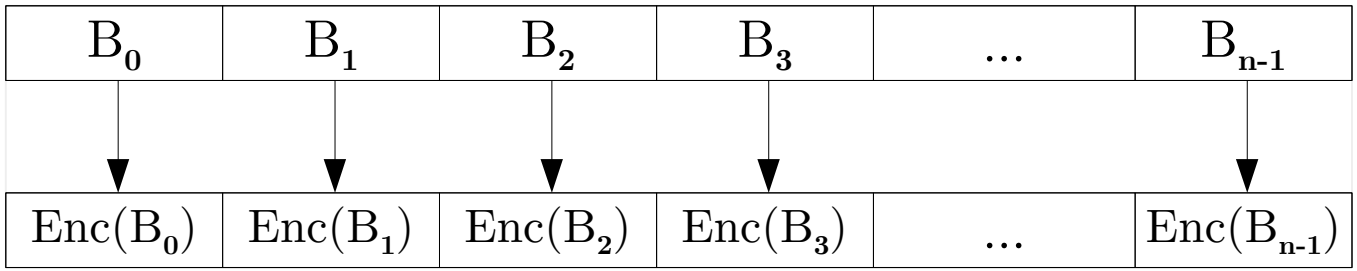

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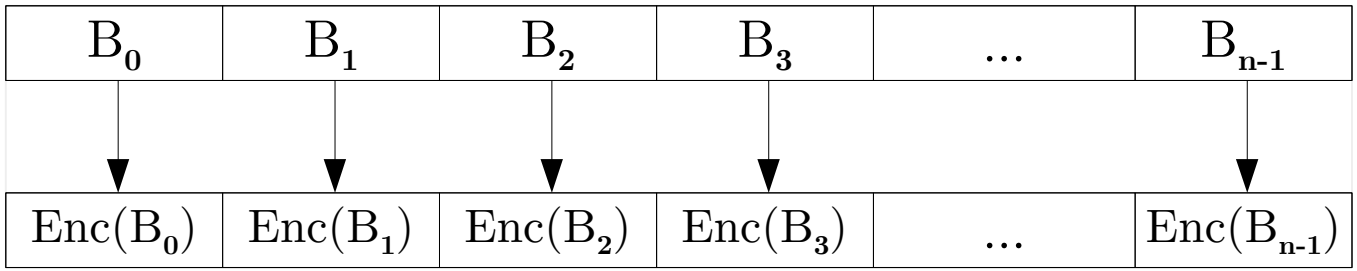

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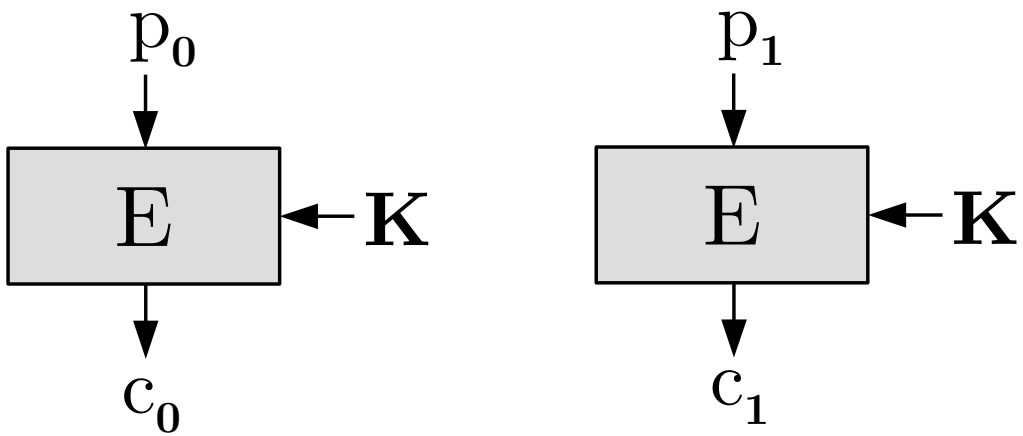

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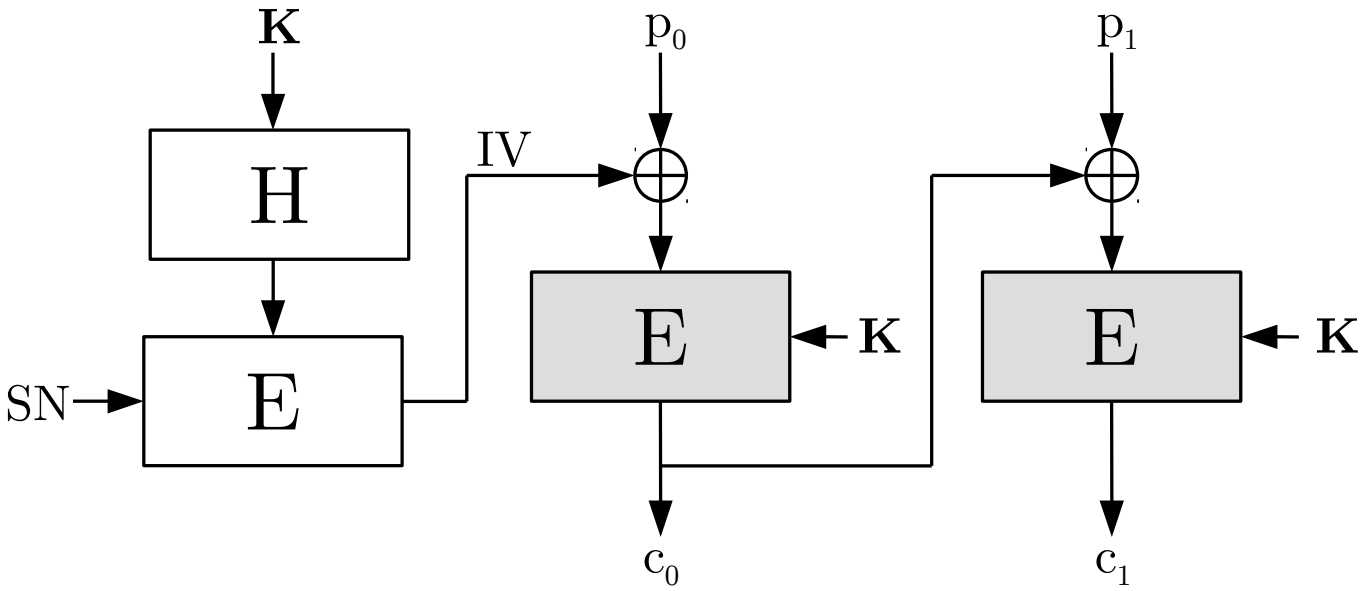

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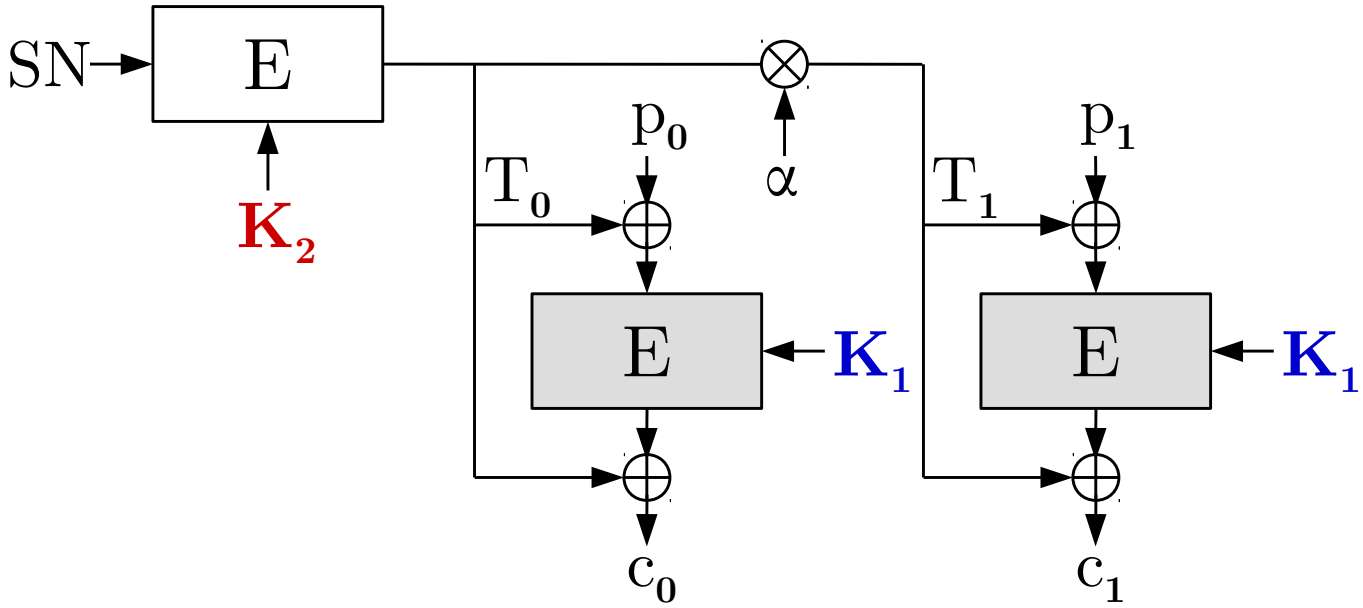

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  - Block ciphers: AES, PRINCE

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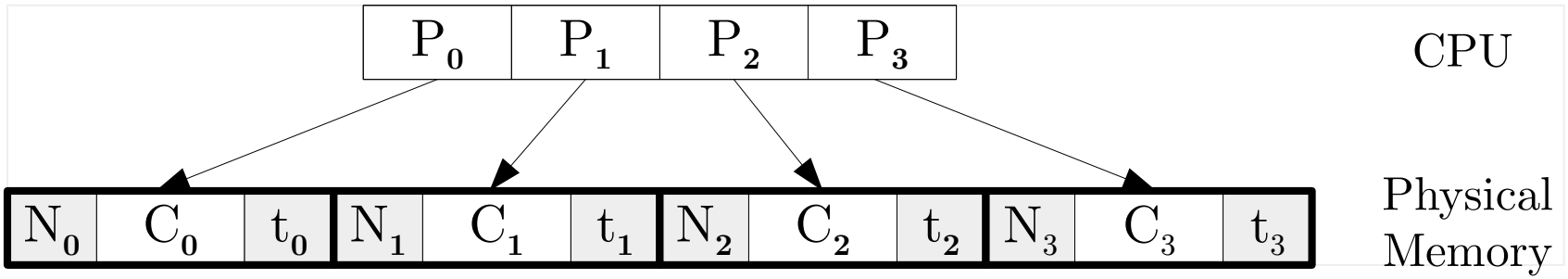

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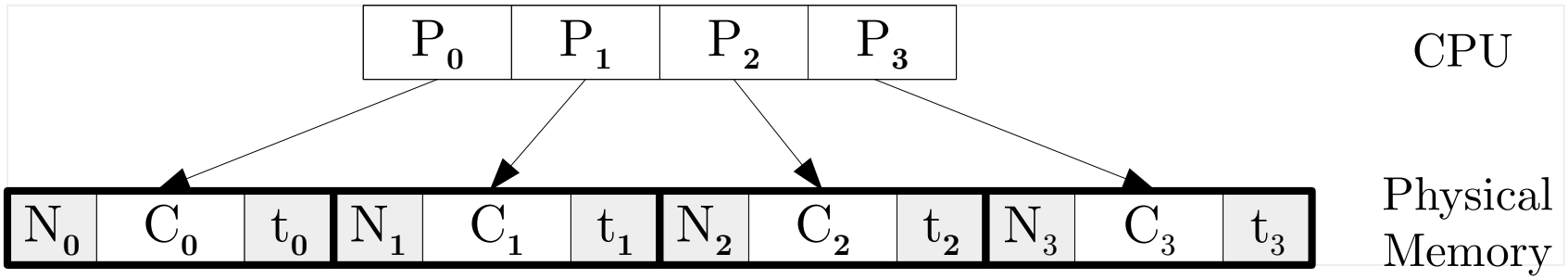

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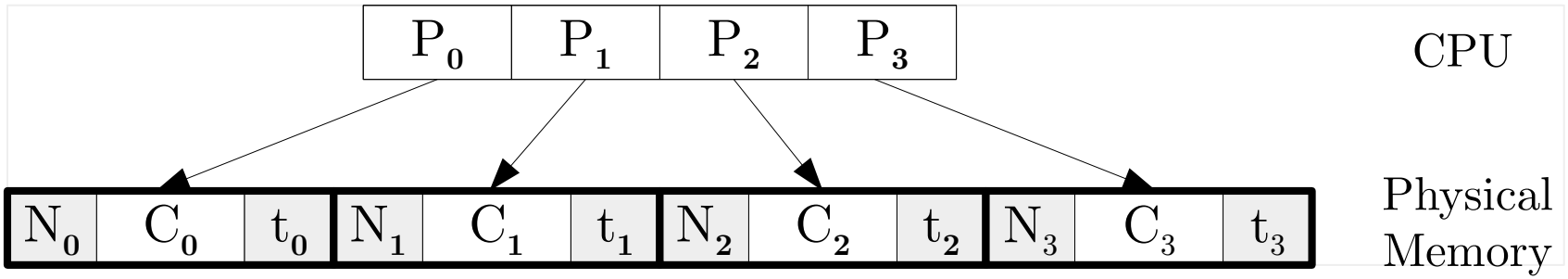
- Attacker cannot create valid $(C, N, t)$ without $K$



# Authentication Trees

- Replay: attacker can restore old data
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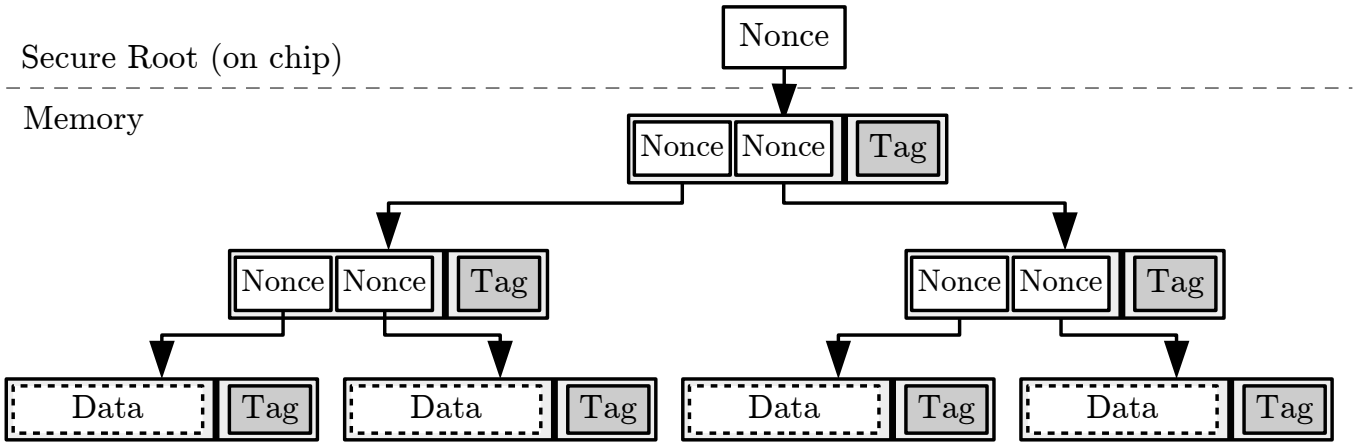
- TEC tree based on ASCON



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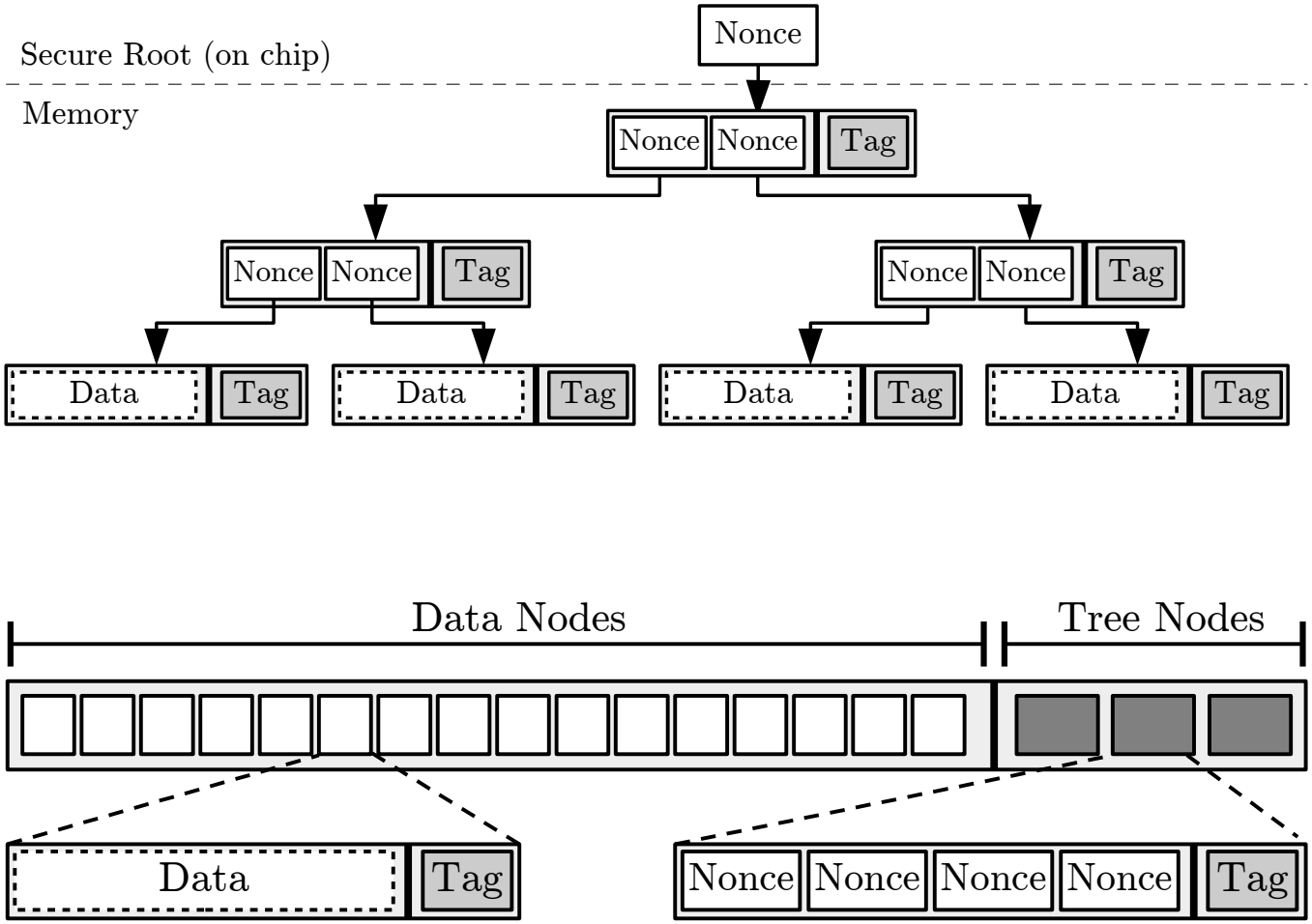
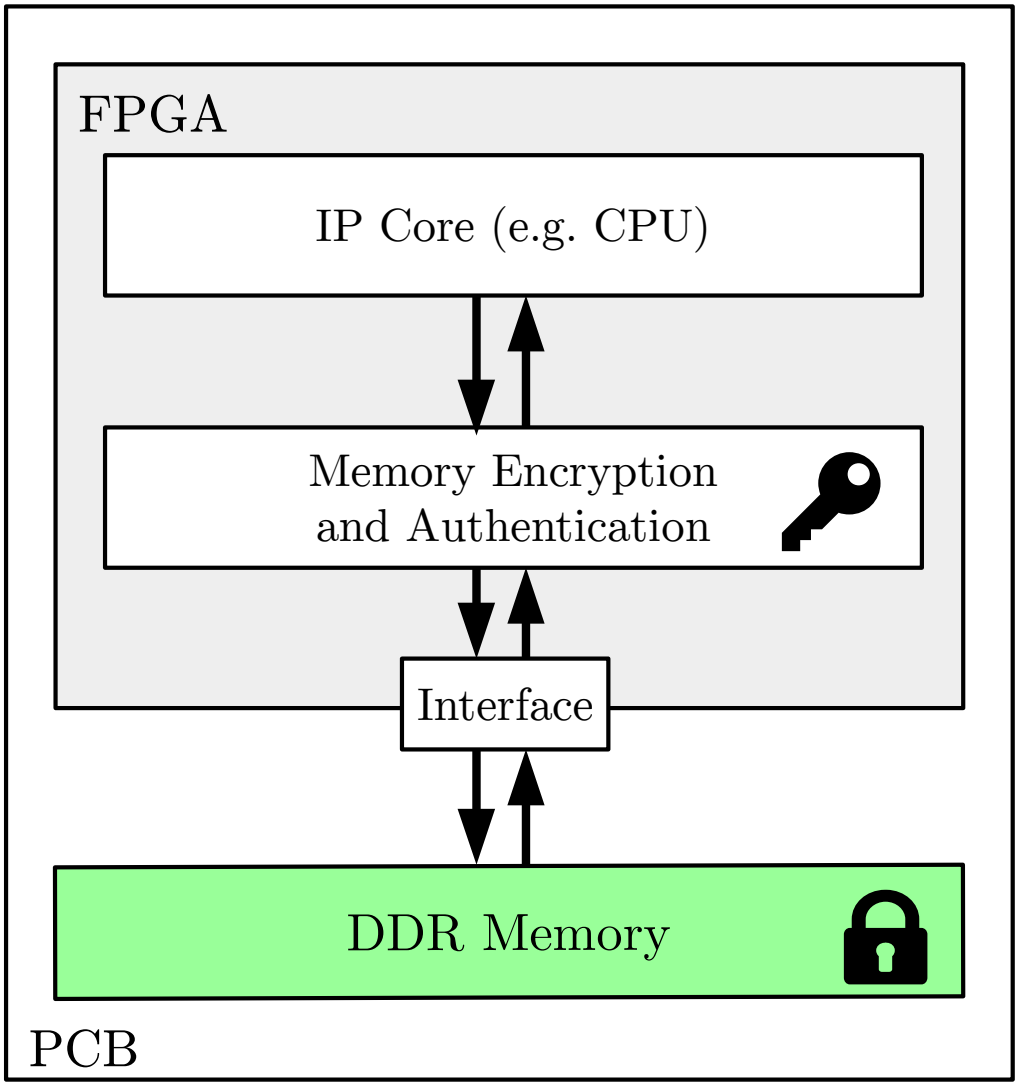


# Implementation



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  - Alignment
  - Block size
  - Metadata (counters, nonces, tags) and layout
- Bus width mismatches
  - Master bus
  - Memory bus
  - Internal data stream
    - Aligned with cryptography

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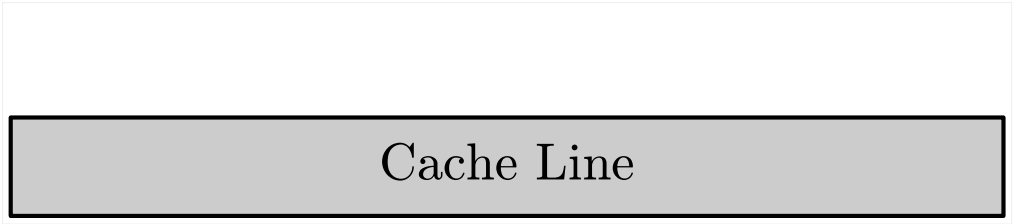

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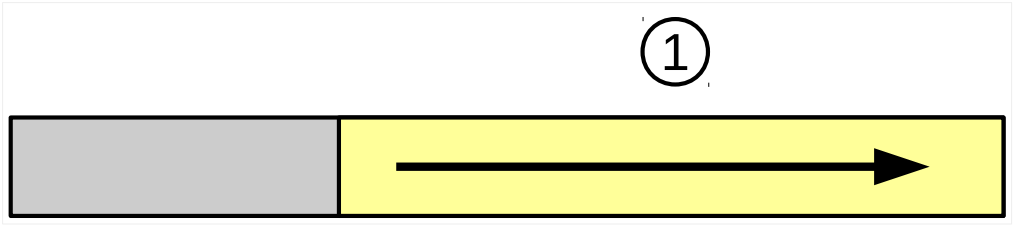

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# Approach

- Framework consisting of modular building blocks
  - Bus interfaces
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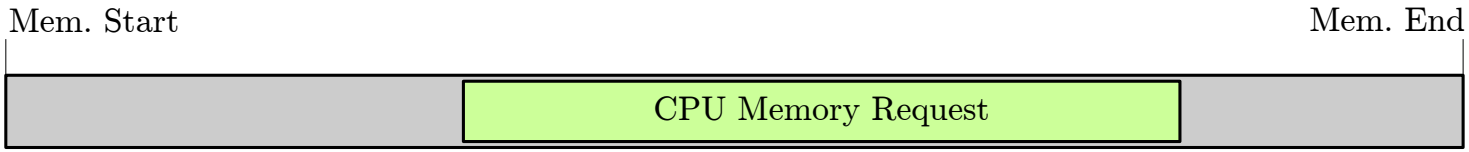
  - Support (synchronization, rate conversions)
- Fully synchronized unidirectional interconnection

# Request Modification



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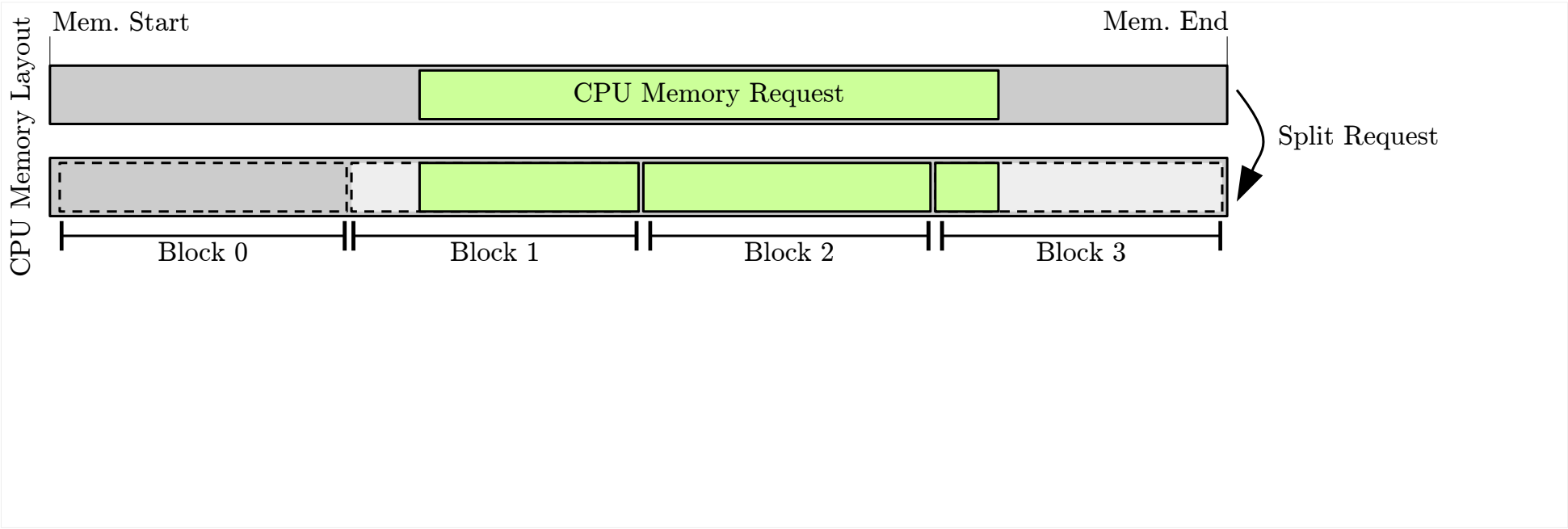

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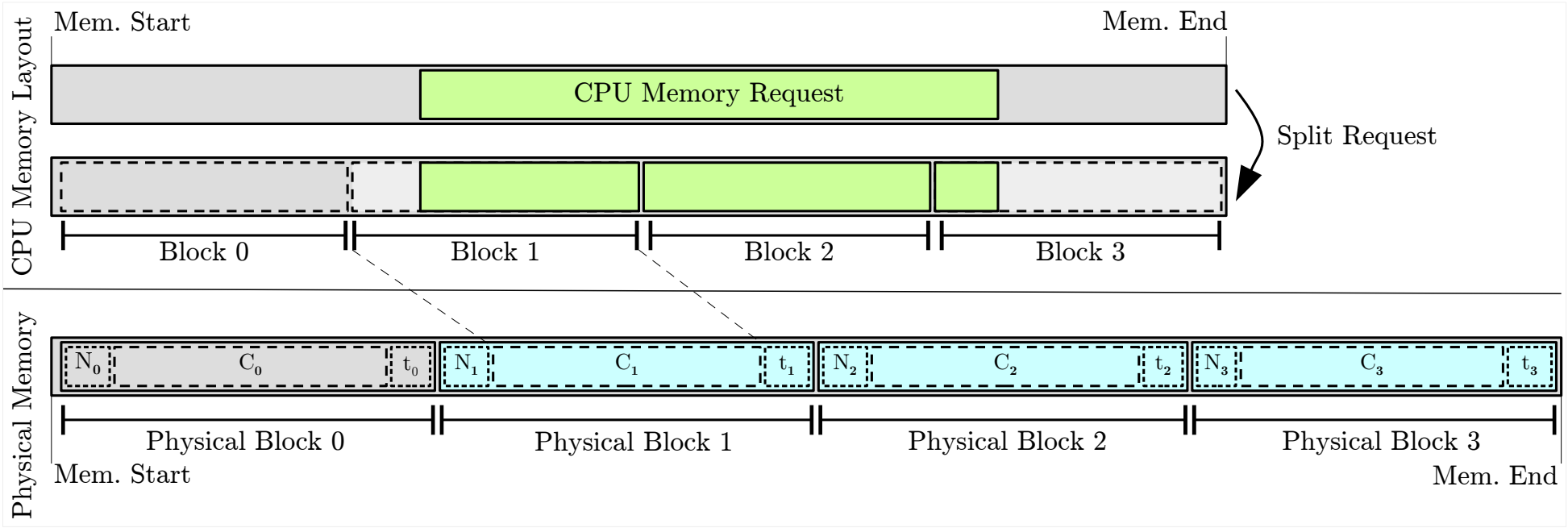
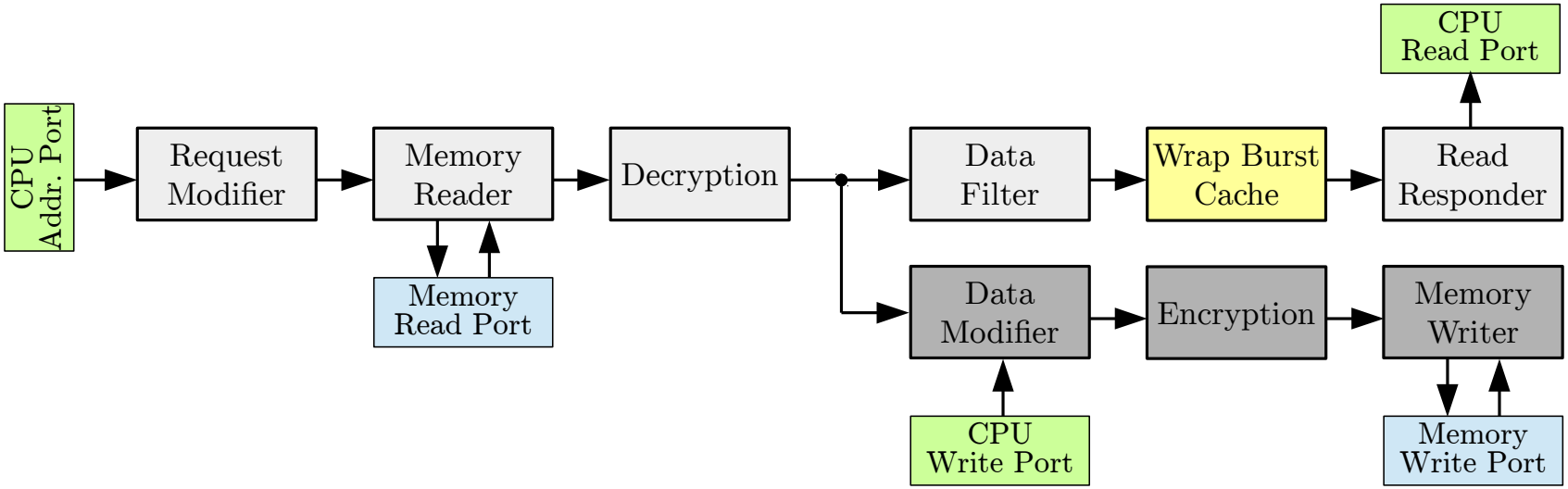
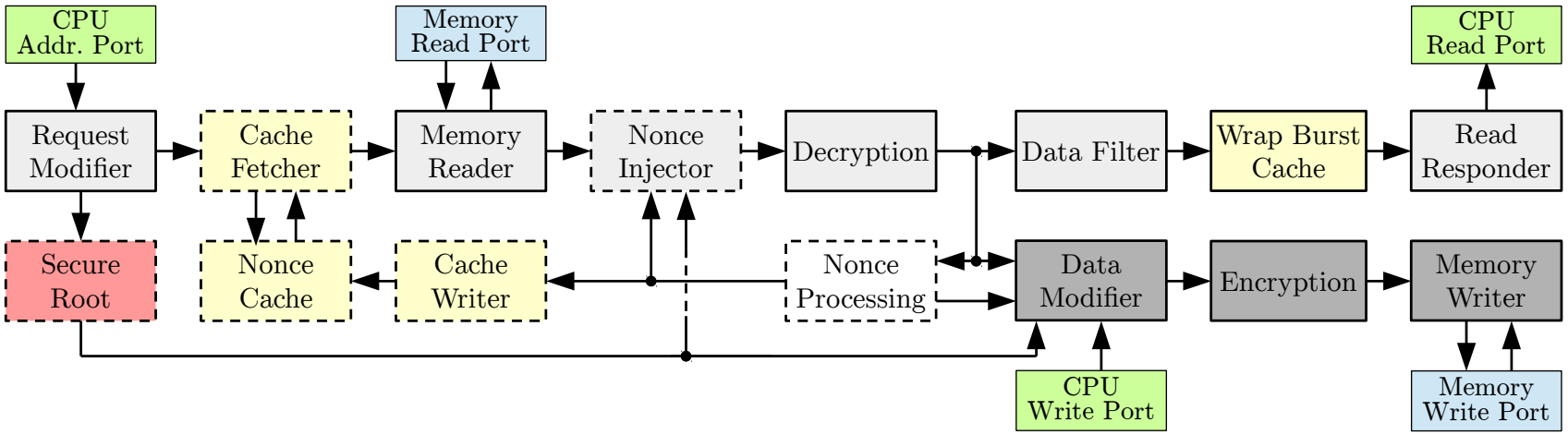


# AXI4 Encryption/Authentication Pipeline



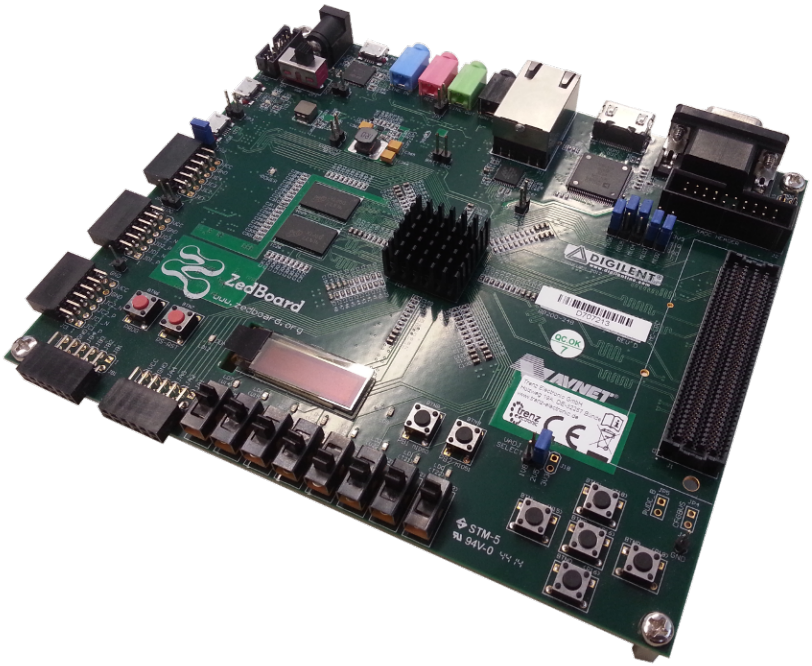

- Writes are always RMW
- Supports block-wise cipher modes (incl. metadata)
- Optimizes wrapping bursts when reading

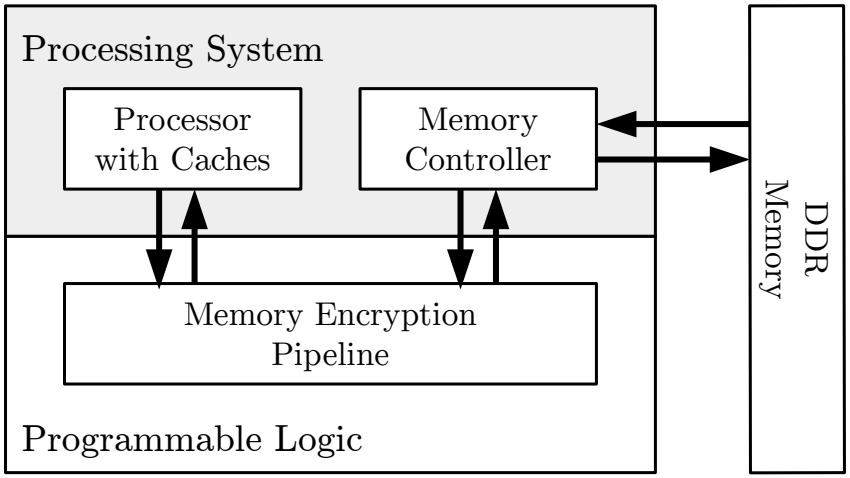
# AXI4 Authentication Tree-Pipeline




- Writes are always RMW
- Single traversal from the root to the leaf
- Speeding it up: caches for read, parallel trees for write
- Arbitrary tree arity

# Evaluation Platform



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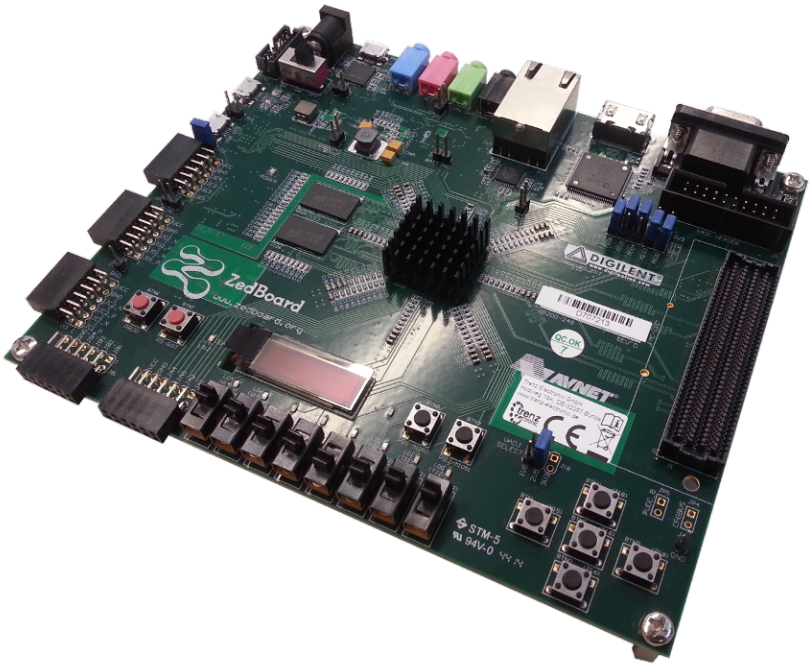


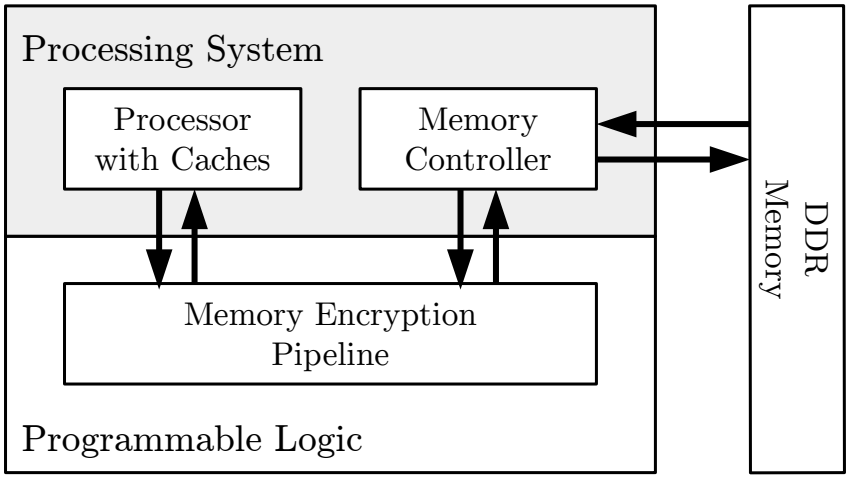


- Block size: cache line

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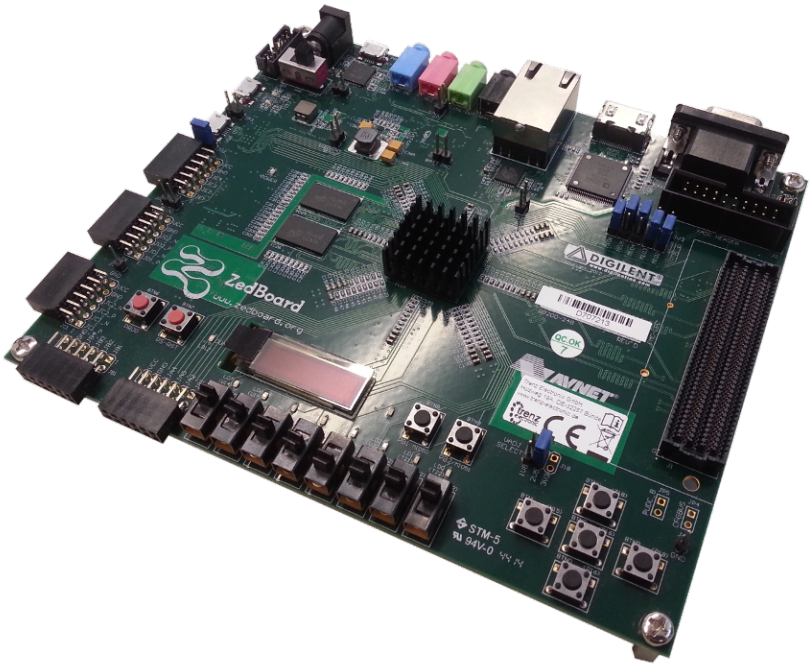
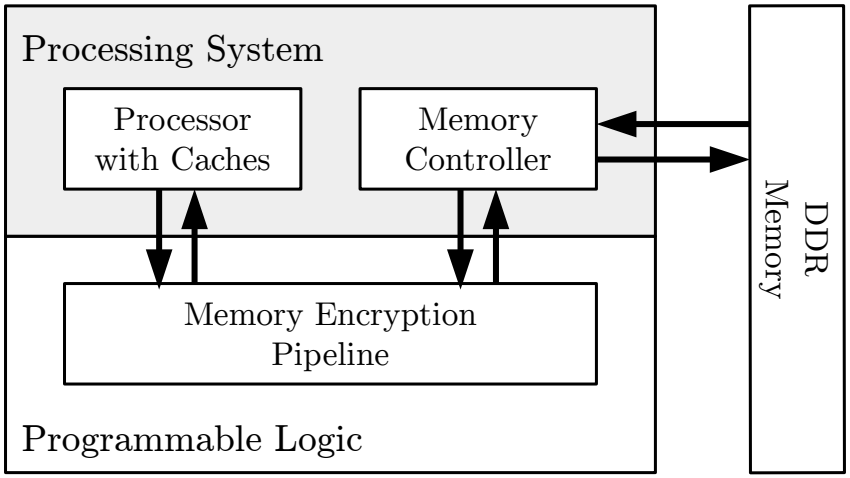
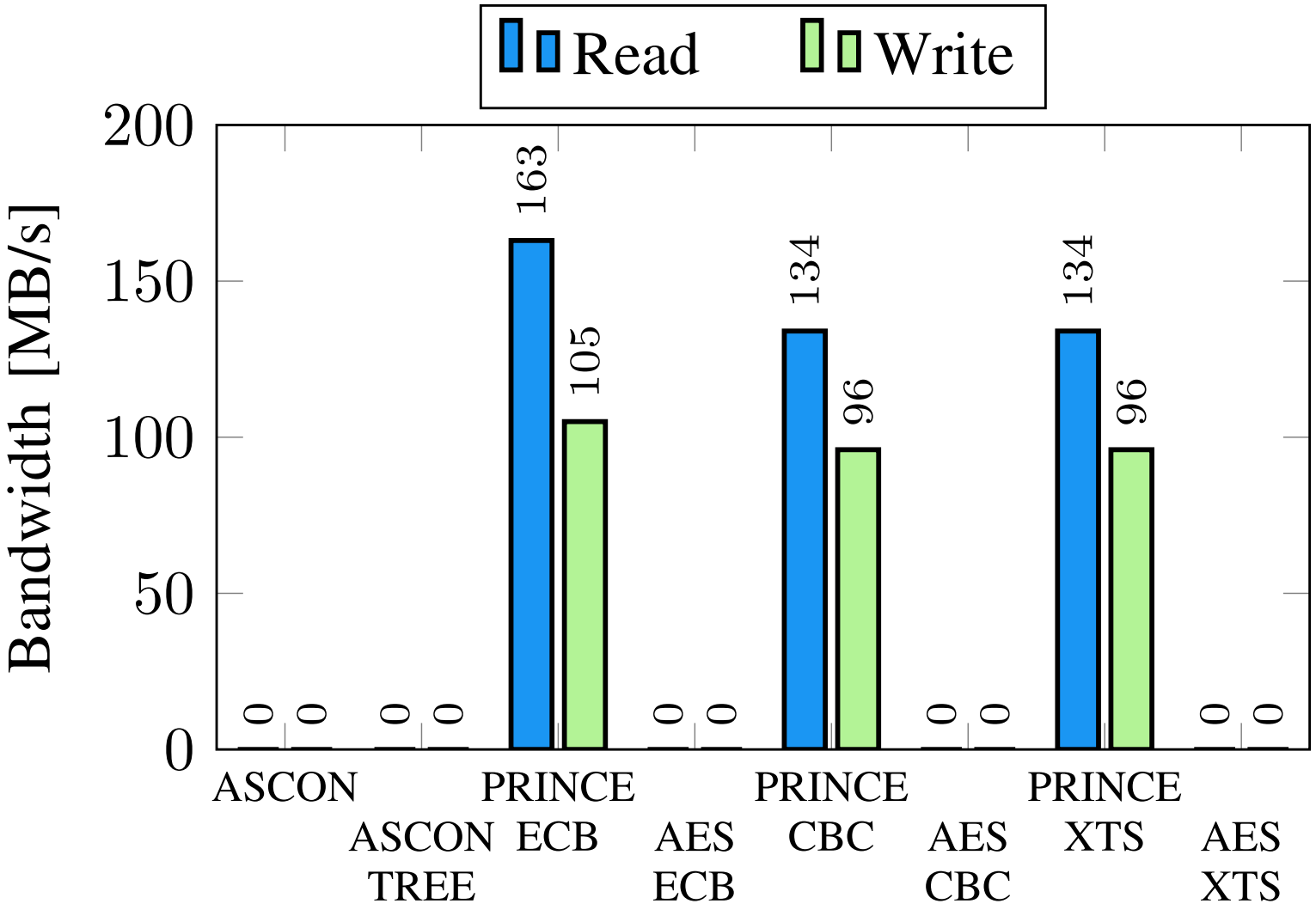



- Block size: cache line
- Running Linux and tinymembench

# Bandwidth @ 50 MHz, 200 MB/s max.



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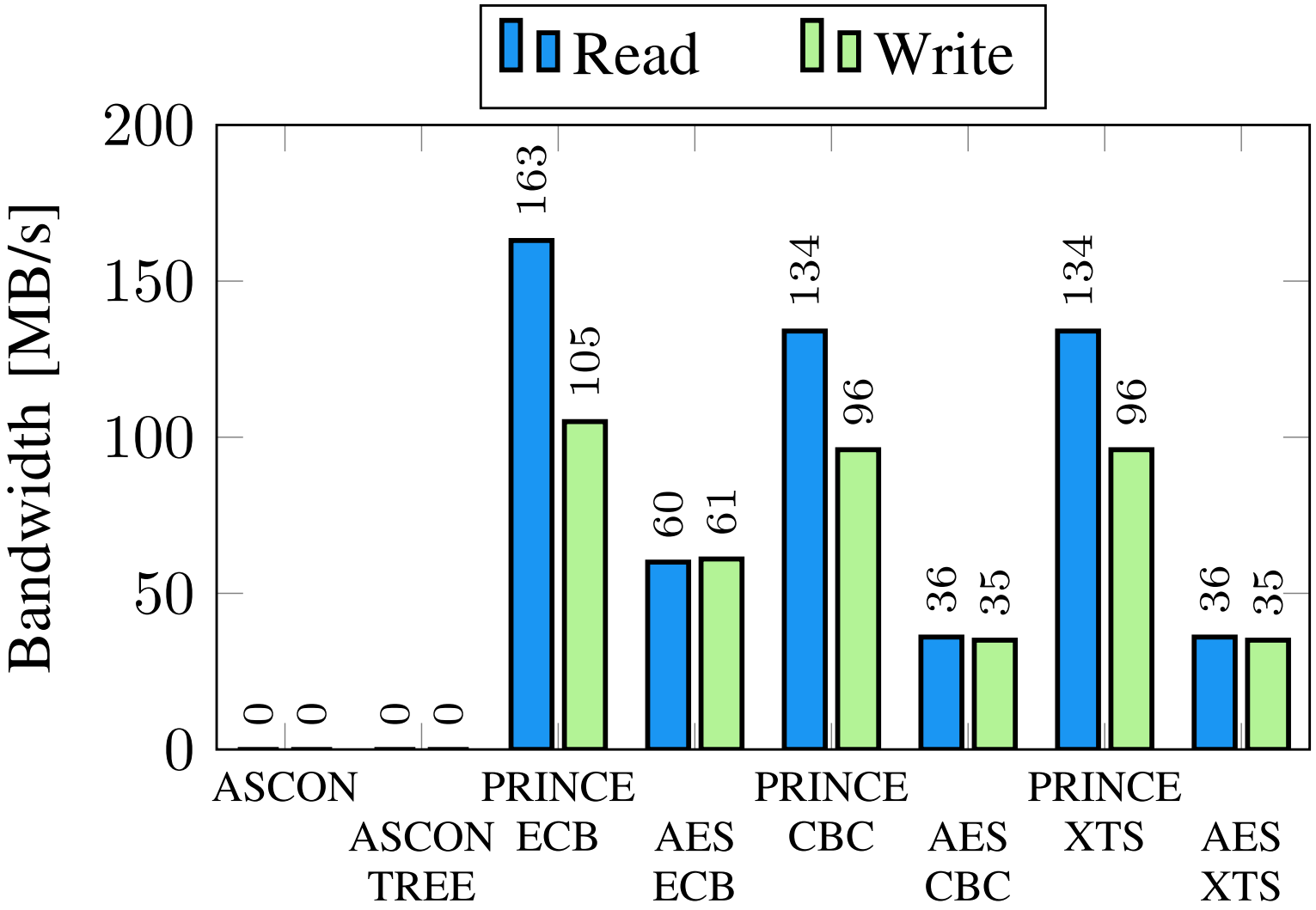

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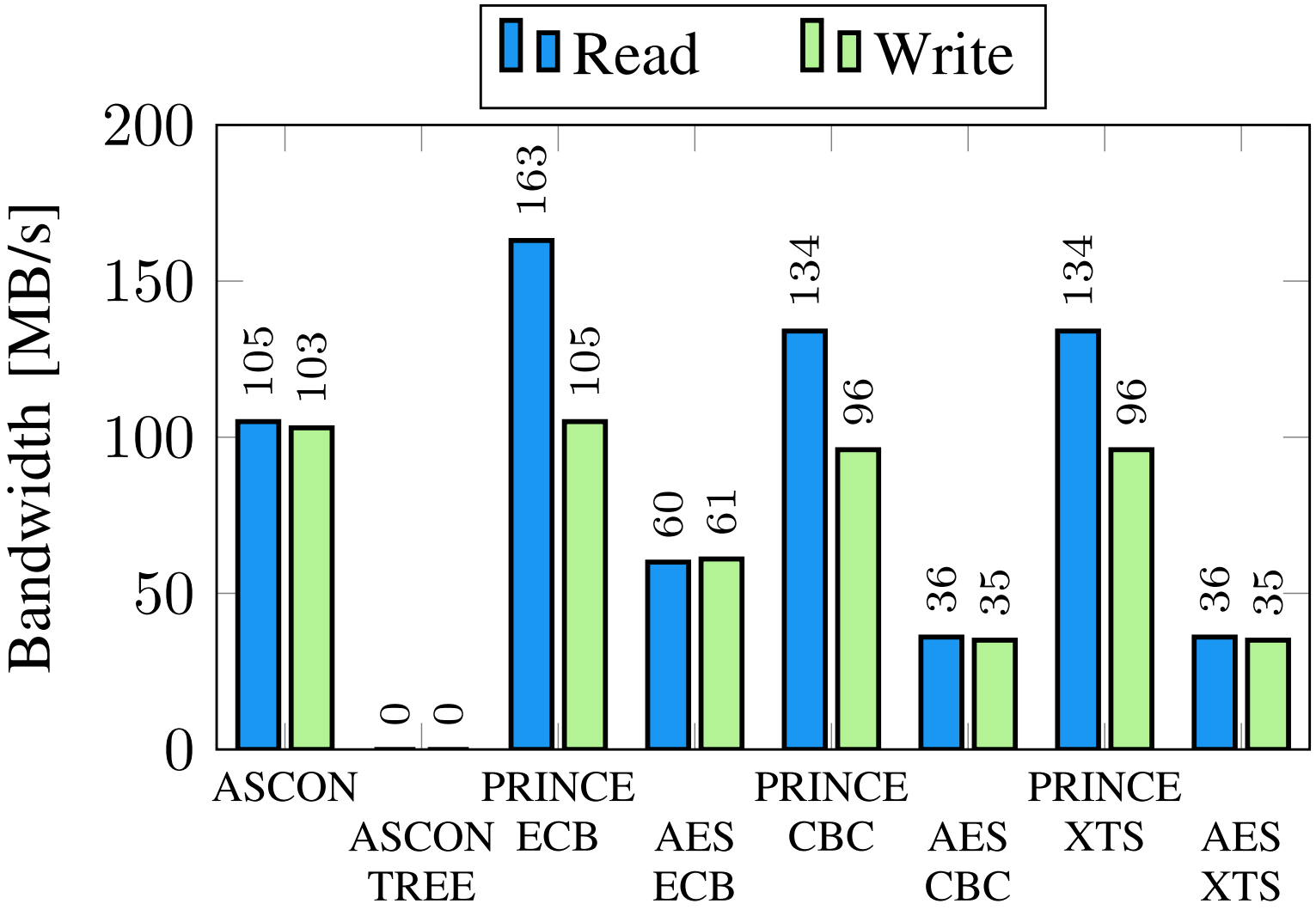

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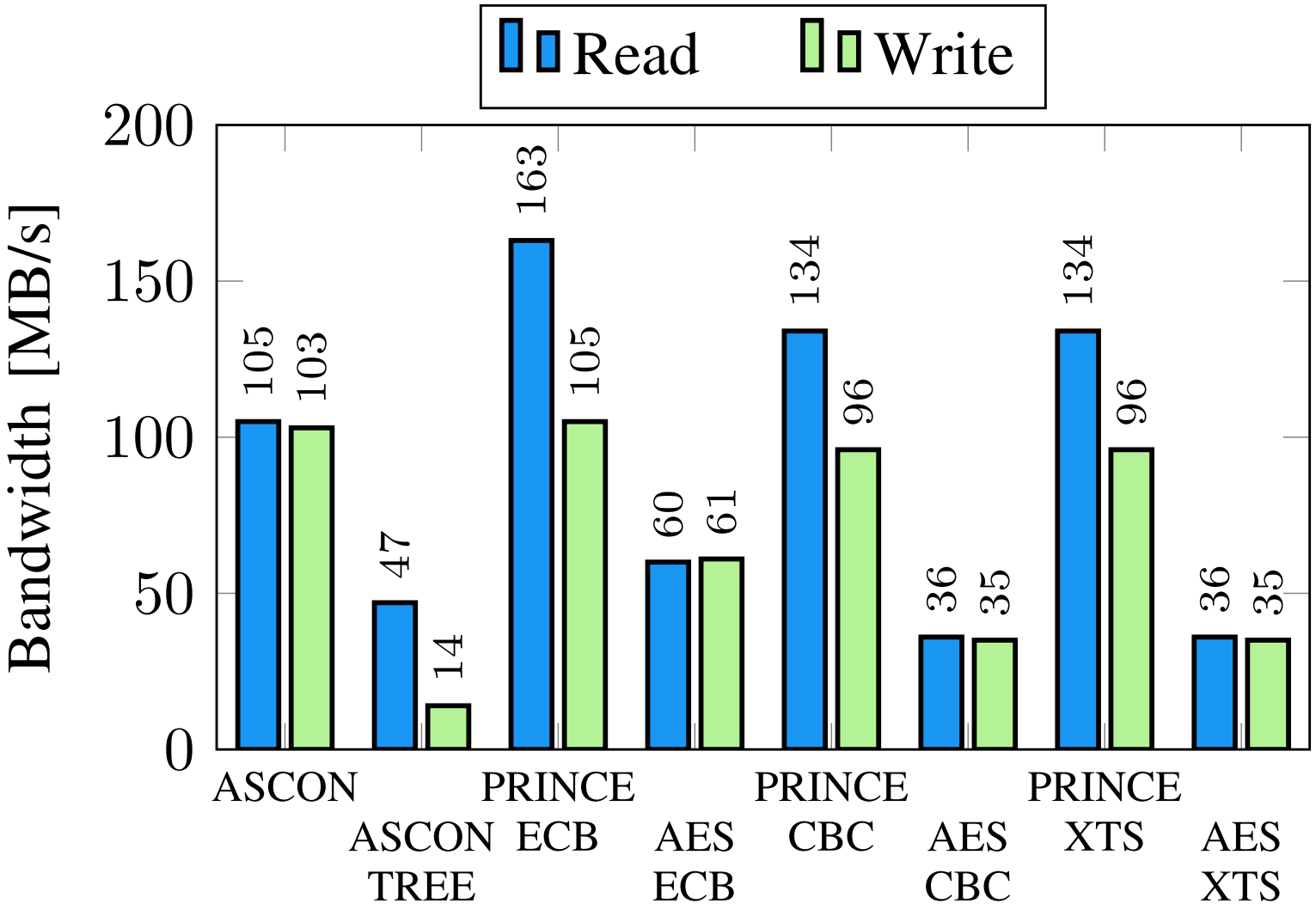

# Conclusion

- Ensure confidentiality and authenticity of data in RAM
- Open-source framework for RAM encryption and authentication
  - Supports various cipher modes: AES/PRINCE, ECB/XTS/CBC, ASCON
  - Tree-based authentication, e.g., ASCON TEC tree
  - Evaluation on Xilinx Zynq-7020 SoC FPGA
  - Efficient pipeline: 94% bandwith utilization
  - ASCON AE for authenticity and efficiency

https://github.com/IAIK/memsec

# Transparent Memory Encryption and Authentication

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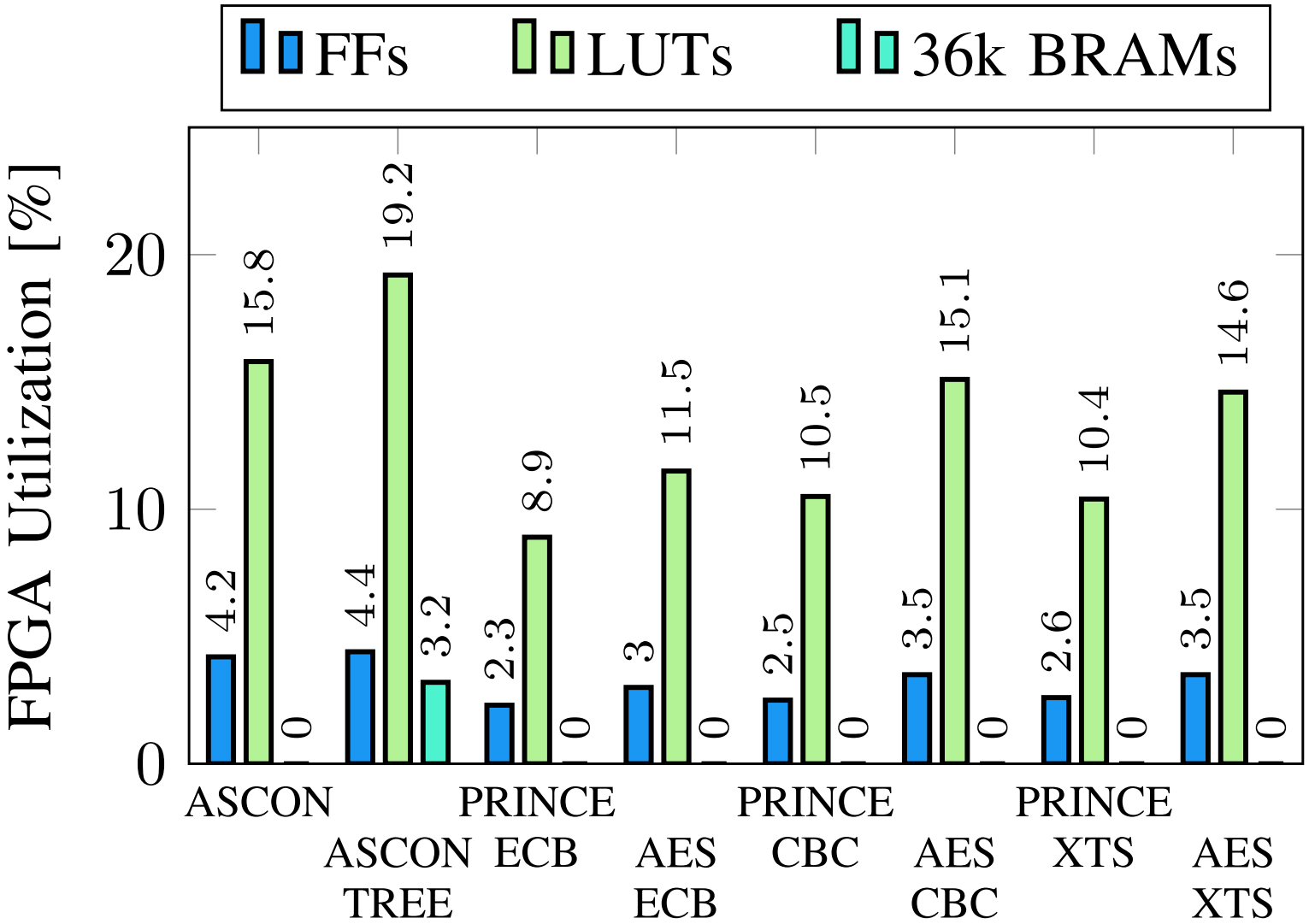
# FPGA Utilization (target: 50 MHz)



# Block Size and Bandwidth (PRINCE CBC)